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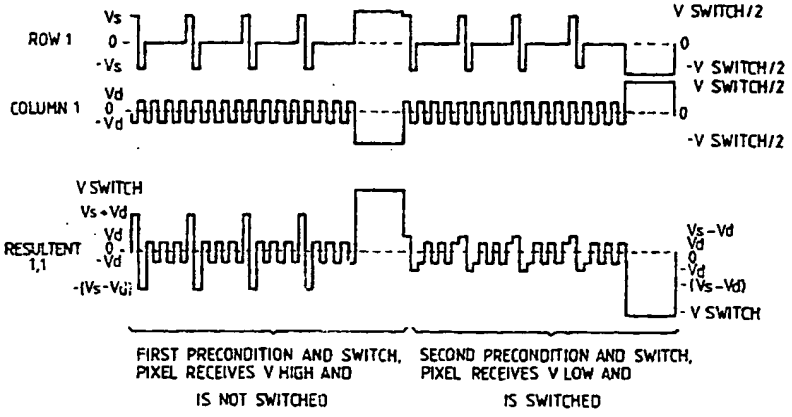

(57) Abstract

The invention concerns a surface stabilised ferroelectric liquid crystal (SSFLC) display devices. Displays are formed by cells containing a thin layer, e.g. 2 μm thick, of smectic liquid crystal material. The cell walls are surface treated and carry e.g. row and column electrodes forming an x,y matrix of addressable display elements or pixels. These devices can show bistability and switch between their two stable state on application of a dc pulse of appropriate polarity, amplitude and width. In this invention the device is addressed by first preconditioning the liquid crystal material at each pixel by applying one of two different levels of ac bias, thereby changing the switching characteristics of the material, and second by switching with application of a switching pulse. This results in pixels that have received the first of the ac bias levels switching whilst the other pixels do not switch. The two levels of ac bias may be applied e.g. by a combination of bipolar strobe pulses and two bipolar data waveforms applied in a multiplex addressing manner to the row and column electrodes. The subsequent switching pulse may be shared between row and column electrodes to give a resultant pulse of appropriate polarity, amplitude and width.

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ADDRESSING FERROELECTRIC LIQUID CRYSTAL DISPLAYS

This invention relates to the addressing of ferroelectric liquid crystal displays.

Liquid crystal display devices are well known. They typically comprise a liquid crystal cell formed by a thin layer of a liquid crystal material held between two glass walls. These walls carry transparent electrodes which apply an electric field across the liquid crystal layer to cause a reorientation of the molecules of liquid crystal material. The liquid crystal molecules in many displays adopt one of two states of molecular arrangement. Information is displayed by areas of liquid crystal material in one state contrasting with areas in the other state. One known display is formed as a matrix of pixels or display elements produced at the intersections between column electrodes on one wall and row electrodes on the other wall. The display is often addressed in a multiplex manner by applying voltages to successive row and column electrodes.

Liquid crystal materials are of three basic types, nematic, cholesteric, and smectic each having a distinctive molecular arrangement.

The present invention concerns ferroelectric smectic liquid crystal materials. Devices using this material form the surface stabilised ferroelectric liquid crystal (SSFLC) device. These devices can show bistability, ie the liquid crystal molecules, more correctly the molecular director, adopt one of two alignment states on switching by positive and negative voltage pulses and remain in the switched state after removal of the voltage. This behaviour depends upon the surface alignment properties.

Some types of surface alignment will produce a device in which the switched states remain after removal of the voltage, other types of surface alignment will produce a device in which the states may randomly decay on removal of the voltage. The switched states may be stabilised by the presence of an ac bias. The actual states achieved may be dependent upon the amplitude of any ac bias present. The ac bias may be provided by the data (column) voltages in a multiplexed device.

There are a number of known systems for multiplex addressing ferroelectric displays; see for example article by Harada et al 1985 S.I.D. Paper 8.4 pp 131-134, and Lagerwall et al 1985 I.D.R.C. pp 213-221. See also GB 2,173,336-A and GB 2,173,629-A. Multiplex addressing schemes for SSFLCs employ a strobe waveform that is applied in sequence to rows but not necessarily to successive rows simultaneously with data waveforms applied to eg column electrodes. The time taken to scan down N lines is termed a field time and equals N times the time taken to address each line - the line address time. For some multiplex modes two field times are required to switch all the pixels to the required state; the total time to completely address a matrix is the frame time. A characteristic of SSFLCs is that they switch on receipt of a pulse of suitable voltage amplitude and length of time of application, ie pulse width, termed a voltage time product V.t. Thus both amplitude and pulse width need to be considered in designing multiplex addressing schemes.

The bistability property, together with the fast switching speed, makes SSFLC devices suitable for large displays with a large number of pixels or display elements. Such ferroelectric displays are described for example in:- N A Clark and S T Lagerwall, Applied Physics Letters Vol 36, No 11 pp 889-901, June, 1980; GB-2,166,256-A; US-4,367,924; US-4,563,059; patent GB-2,209,610 [Bradshaw and Raynes]; R B Meyer et al, J Phys Lett 36, L69, 1975.

For displays having a large number N the time taken by two field times can be significant. One way of reducing this is to blank all pixels to one state with a single blanking pulse, then scan each line with a strobe pulse during one field time to switch selected pixels to the other state. In this case the total time to address is one field time. A disadvantage of whole frame blanking is display appearance, and loss of information whilst the blanked display is being written. Alternatively the blanking pulse may also scan the lines preceding the strobe pulse by, eg five lines. In this method there is no degradation of display appearance.

Although the SSFLC offers fast switching times and thus the possibility of complex displays there is still a need for increased switching speed to permit the introduction of grey scale and colour. Grey scale requires temporal or spatial dither; colour requires subpixellation to a triplet for each pixel or frame sequential introduction of the primary colours. Each of these techniques requires an improved scanning rate, either to maintain flicker free frame rates with the introduction of subframes (temperal dither and frame sequential) or to cope with the increased number of pixels from subpixellation (spatial dither and colour triplets).

The problem of lengthy addressing time and display appearance is solved according to this invention by preconditioning pixels prior to applying a switching voltage time product to all or a plurality of the pixels at once, so that only selected pixels change state when the switching voltage time product is applied.

According to this invention a method of multiplex addressing a ferroelectric liquid crystal display formed by the intersections of an m set of electrodes and an n set of electrodes across a layer of smectic liquid crystal material to provide an m x n matrix of addressable pixels comprises the steps of:

generating row and column waveforms comprising voltage pulses of various dc amplitude and sign for applying to the m and n sets of electrodes;

addressing the m and n set of electrodes with the row and column waveforms applied through driver circuits to address each pixel;

characterised by the steps of:-

preconditioning the liquid crystal material at each pixel by applying two different levels of ac bias to the pixels, a first level at pixels required to be switched and a second level to the other pixels;

applying a dc switching pulse to all m and n electrodes associated with the pixels required to be switched;

whereby all pixels required to be switched are switched by the dc switching pulse to the required state and other pixels remain unswitched.

According to this invention a multiplex addressed liquid crystal display comprises:

a liquid crystal cell including a layer of ferroelectric smectic liquid crystal material contained between two walls, an m set of electrodes on one wall and a n set of electrodes on the other wall arranged to form collectively an m,n matrix of addressable pixels;

waveform generators for generating m and n waveforms of unidirectional pulses in successive time slots (ts) for applying the waveforms to the m and n set of electrodes through driver circuits;

means for controlling the application of m and n waveforms so that a desired display pattern is obtained,

characterised by:-

means for applying a first or a second of two different levels of ac bias at each pixel;

means for generating switching pulses for applying to the m and n set of electrodes and for applying a switching pulse at each pixel required to be switched;

whereby each pixel required to be switched is preconditioned by application of the first of the two levels of ac bias whilst other pixels receive the second level of ac bias, and the subsequent application of the switching pulse switches only those pixels preconditioned by application of the first ac bias so that a required pattern of pixels is displayed.

Techniques for producing waveforms to generate two different levels of ac bias at selected pixels in a matrix display are well known from their use with twisted nematic (TN) and supertwisted nematic displays (STN). See, eg, P M Alt and P Pleshko, IEEE Trans Electron Devices ED-21, 146-155, 1978; J Nehring and A Kmetz, IEEE Trans Electron Devices, ED-26, 785-802, 1979; M G Clark, I A Shanks and N J Patterson, Proc SID Int Sump Digest, 1979, paper 13-1, pp 110-111.

In addition to the widely used "Alt and Pleshko" waveforms other suitable waveforms include pseudo random binary sequences and Walsh function, as used eg in T J Scheffer and B Clifton, Proc SID Int Symp Digest, 1992, paper 13-4, pp 228-231.

The two different levels of ac bias may be obtained at each pixel by the resultant of row and column waveforms addressing the electrodes in a multiplex manner. The switching pulse may be applied to all electrodes simultaneously. The switching pulse may be split in magnitude between the two sets of electrodes.

The frequency of the ac bias is sufficiently high to affect the switching characteristic of the smectic material without causing switching in the absence of a switching pulse.

Brief description of drawings:

One form of the invention will now be described, by way of example only, with reference to the accompanying drawings in which:-

Figures 1, 2, are plan and section views of a liquid crystal display device;

Figure 3 is a stylised sectional view of part of Figure 2 to a larger scale, showing one of several possible director profiles;

Figure 4 is a graph showing switching characteristics of pulse width against pulse voltage for different levels of AC bias;

Figure 5 shows a 4 x 4 x,y matrix with a display pattern, together with waveforms for applying to the x,y electrodes to generate two different levels of ac bias at different pixels;

Figure 6 shows waveforms for one row and one column, plus the resultant waveform at their intersection for several cycles required to precondition the pixels, followed by a switching pulse at the end of this preconditioning period.

Description of preferred embodiments.

The cell 1 shown in Figures 1, 2 comprises two glass walls, 2, 3, spaced about 1-6 μm apart by a spacer ring 4 and/or distributed spacers. Electrode structures 5, 6 of transparent indium tin oxide are formed on the inner face of both walls. These electrodes may be of conventional row (x) and column (y) shape, seven segment, or an r-θ display. A layer 7 of liquid crystal material is contained between the walls 2, 3 and spacer ring 4. Polarisers 8, 9 are arranged in front of and behind the cell 1. The alignment of the optical axis of the polarisers 8, 9 are arranged to maximise contrast of the display; ie approximately crossed polarisers with one optical axis along one switched molecular direction. A d.c. voltage source 10 supplies power through control logic 11 to driver circuits 12, 13 connected to the electrode structures 5, 6, by wire leads 14, 15.

The device may operate in a transmissive or reflective mode. In the former light passing through the device e.g. from a tungsten bulb 16 is selectively transmitted or blocked to form the desired display. In the reflective mode a mirror 17 is placed behind the second polariser 9 to reflect ambient light back through the cell 1 and two polarisers. By making the mirror 17 partly reflecting the device may be operated both in a transmissive and reflective mode with one or two polarisers.

Prior to assembly the walls 2, 3 are surface treated eg by spinning on a thin layer of a polymer such as a polyamide or polyimide, drying and where appropriate curing; then buffing with a soft cloth (e.g. rayon) in a single direction R1, R2. This known treatment provides a surface alignment for liquid crystal molecules. The molecules (as measured in the nematic phase) align themselves along the rubbing direction R1, R2, and at an angle of about 0° to 15° to the surface depending upon the polymer used and its subsequent treatment; see article by S Kuniyasu et al, Japanese J of Applied Physics vol 27, No 5, May 1988, pp827-829. Alternatively surface alignment may be provided by the known process of obliquely evaporating eg. silicon monoxide onto the cell walls.

The surface alignment treatment provides an anchoring force to adjacent liquid crystal materials molecules. Between the cell walls the molecules are constrained by elastic forces characteristic of the material used. The material forms itself into molecular layers 20 each parallel to one another as shown in Figure 3 which is a specific example of many possible structures. The Sc is a tilted phase in which the director lies at an angle to the layer normal, hence each molecular director 21 can be envisaged as tending to lie along the surface of a cone, with the position on the cone varying across the layer thickness, and each macro layer 20 often having a chevron appearance.

Considering the material adjacent the layer centre, the molecular director 21 lies approximately in the plane of the layer. Application of a dc voltage pulse of appropriate sign will move the director along the cone surface to the opposite side of the cone. The two positions D1, D2 on this cone surface represent two stable states of the liquid crystal director, ie the material will stay in either of these positions D1, D2 on removal of applied electric voltage.

In practical displays the director may move from these idealised positions. It is common practice to apply an ac bias to the material at all times when information is to be displayed. This ac bias has the effect of moving the director and can improve display appearance. The effect of ac bias is described for example in Proc 4th IDRC 1984 pp 217-220. Display addressing scheme using ac bias are described eg in GB patent application number 90.17316.2, PCT/GB 91/01263, J R Hughes and E P Raynes. The ac bias may be data waveforms applied to the column electrodes 15.

Figure 4 shows the switching characteristics for the material SCE8. The curves mark the boundary between switching and nonswitching; switching will occur for a pulse voltage time product above the line. As shown the lower curve is obtained for an applied ac bias of 7.5 volts, and the upper curve for 12.5 volts. These characteristics were obtained at an ac frequency of 50 kHz.

Between the two curves a suitable switching voltage and pulse width is marked, ie 30v for 130μs.

Figure 5 shows one technique whereby preconditioning ac voltage levels are applied to a simple 4 x 4 pixel display. This is one implementation of the Alt and Pleshko waveforms. Dark circles represent pixels which will receive a higher level of ac bias (and therefore do not switch) and the open circles represent pixels which will receive a lower level of ac bias (and therefore will switch).

To obtain this preconditioning pattern, a strobe waveform is applied to each row R1 to R4 in turn. The strobe has pulses of +Vs in one time slots (ts) and -Vs in the next ts, followed by 6ts of zero voltage.

Data waveforms are applied to each column or y-electrode. Data waveforms are alternate pulses of +Vd and -Vd, each lasting one time slot. The data waveform for a pixel that is to receive a higher level of ac bias is 180° out of phase with the data waveform for a pixel that receives the lower level of ac bias.

The Alt and Pleshko relationships give the ratio of higher level of ac bias to lower level of ac bias:

$$V_{high}/V_{low} = M = (/N +1 / /N -1)^{\frac{1}{2}}$$

where N = number of scanned lines.

Therefore in the simple four row example of Figure 5,
$V_{high}/V_{low} = 1.732$.

The ratio of Vs : Vd is given by Vs = /N Vd, and therefore Vs = 2Vd.

The value of Vd is given by:

$$Vd = \tfrac{1}{2}(M^2 + 1)^{\frac{1}{2}} * V_{low},$$

$$Vd = V_{low}, \text{ and } Vs = 2*V_{low}$$

Hence the values of Vs and Vd are arrived at from a knowledge of the the switching characteristic shown in Figure 4.

The width of ts is determined by:- the length of time the preconditioning waveform is required to be applied; the need to apply several cycles of the preconditioning waveform to ensure that the required rms value is experienced by the liquid crystal material; and the need to keep the ac frequency content high to prevent partial switching of the liquid crystal material director to the ac component.

The strobe, data, and resultant waveforms for one intersection, R1C1, are shown in Figure 6 for a single frame time of two field times. The strobe waveform comprises bipolar pulses of +Vs for 1ts immediately followed by -Vs for 1ts, then zero volts for 6ts repeated four times, and ending with a long pulse of Vswitching/2 for 7ts forming a first field time. This is followed by an identical waveform for the second field time, ending in a single long pulse of -Vswitching for 7ts. The column waveforms in the first field are bipolar pulses of -/+Vd each pulse lasting 1ts, and ending in a single long pulse of -Vswitching/2. In the second field time the column waveform is the inverse of that during the first field time, ie +/- Vd ending in a single long pulse of +Vswitching/2 for 7ts.

During the first field time the resultant contains voltage excursions to +/- (Vs+Vd) amongst pulses of +/- (Vd); the rms value of this first field time is arranged to be 12.5 volts. During the second field time the resultant has voltage pulses of +/- (Vs-Vd) and +/- (Vd); the rms value of this is arranged to be 7.5volts. The resultant of the +/-Vs and +/-Vd waveforms do not switch the display, they merely precondition the smectic material to accept a switching pulse of suitable time-voltage product.

Pixels where an ac bias of 12.5v have been applied will switch as shown in the upper curve of Figure 4, whilst the other pixels which have received the ac bias of 7.5v will switch as shown in the lower curve. Thus a resultant switching pulse of +Vswitching for 7ts shown at the end of the first field waveforms in Figure 6 will not switch the pixel R1C1 because that pixel has been preconditioned with 12.5v. However, R1C1 will switch on receipt of the -Vswitching for 7ts shown at the end of the second field because this pixel has just been preconditioned with 7.5v ac.

The material SCE8 has been found to require application of ac bias for about 1.0ms to precondition the material to switch.

To obtain a Vhigh : Vlow ratio of 12.5 : 7.5 the Alt and Pleshko relationships show that only 4 rows may be preconditioned simultaneously:-

$$N = \{(M^2+1)/(M^2-1)\}^2 \text{ where } M = Vhigh/Vlow$$

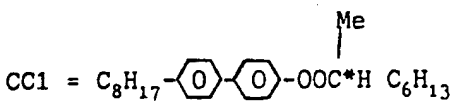
It has been found that for the material SCE8 at 25°C, a switching pulse of 45v for 132μs may be used with preconditiong ac voltages of 6.0v and 9.0v. The row waveform has Vs = 13.2v, and column waveforms Vd = 5.4v, with ts = 12μs. This allows 6 rows to be preconditioned simultaneously. One cycle of Alt and Pleschko waveforms was thus 6 rows times 2ts times 12μs equal 144μs, and 7 complete cycles can be achieved in the required preconditioning time of about 1ms.

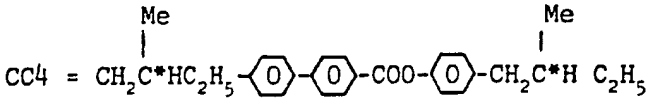
The are a number of variations to the above. For example, immediately prior to the preconditioning waveforms, all pixels could be blanked to the OFF state and then selectively switched to the ON state by the switching pulse. Alternatively, two periods of preconditioning followed by switching are necessary to address all pixels.

Materials which show a minimum in their response time-voltage characteristic (-V minimum) are particularly suited to this application since the higher voltage regime of their -V curves is particularly sensitive to a.c. stabilisation.

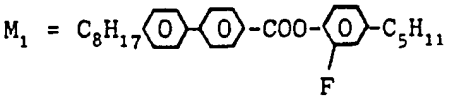
Suitable materials include catalogue references SCE 8, ZLI-5014-000, available from Merck Ltd, those listed in PCT/GB88/01004, WO 89/05025, and:-

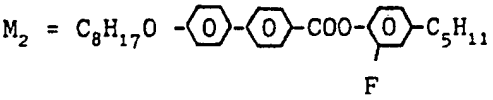
19.6% CM8 (49% CC1 + 51% CC4) + 80.4% H_1

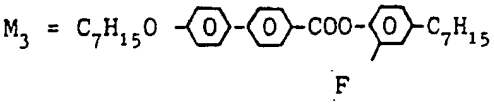
CC1 = 

CC4 = 

$H_1 = M_1 + M_2 + M_3$ (1 : 1 : 1)

M_1 = 

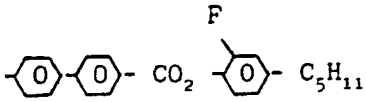
M_2 = 

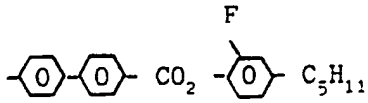
M_3 = 

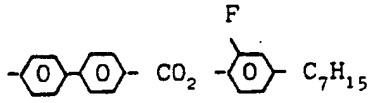
Another mixture is LPM 68 = H1 (49.5%), AS 100 (49.5%), IGS 97(1%)

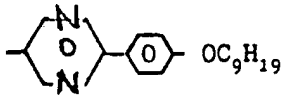
H1 = MB 8.5F + MB 80.5F + MB 70.7F (1 : 1 : 1)

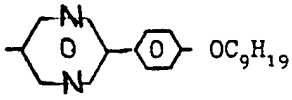
AS100 = PYR 7.09 + PYR 9.09 (1 : 2)

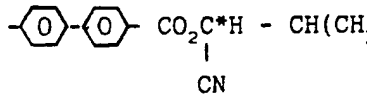
MB 8.5F = C_8H_{17}  C_5H_{11}

MB 80.5F = $C_8H_{17}O$  C_5H_{11}

MB 70.7F = $C_7H_{15}O$  C_7H_{15}

PYR 7.09 = C_7H_{15}  OC_9H_{19}

PYR 9.09 = C_9H_{19}  OC_9H_{19}

IGS 97 = $C_8H_{17}O$  $CO_2C^*H(CN) - CH(CH_3)_2$

Claims:

1. A method of multiplex addressing a ferroelectric liquid crystal display formed by the intersections of an m set of electrodes and an n set of electrodes across a layer of smectic liquid crystal material to provide an m x n matrix of addressable pixels comprising the steps of:-

generating row and column waveforms comprising voltage pulses of various dc amplitude and sign for applying to the m and n sets of electrodes;

addressing the m and n set of electrodes with the row and column waveforms applied through driver circuits to address each pixel;

characterised by the steps of:-

preconditioning the liquid crystal material at each pixel by applying two different levels of ac bias to the pixels, a first level at pixels required to be switched and a second level to the other pixels;

applying a dc switching pulse to all m and n electrodes associated with the pixels required to be switched;

whereby all pixels required to be switched are switched by the dc switching pulse to the required state and other pixels remain unswitched.

2. A multiplex addressed liquid crystal display comprising:-

a liquid crystal cell including a layer of ferroelectric smectic liquid crystal material contained between two walls, an m set of electrodes on one wall and a n set of electrodes on the other wall arranged to form collectively an m,n matrix of addressable pixels;

waveform generators for generating m and n waveforms comprising voltage pulses of various dc amplitude and sign in successive time slots (ts) and applying the waveforms to the m and n set of electrodes through driver circuits;

means for controlling the application of m and n waveforms so that a desired display pattern is obtained,

characterised by:-

means for applying a first or a second of two different levels of ac bias at each pixel;

means for generating switching pulses for applying to the m and n set of electrodes and for applying a switching pulse at each pixel required to be switched;

whereby each pixel required to be switched is preconditioned by application of the first of the two levels of ac bias whilst other pixels receive the second level of ac bias, and the subsequent application of the switching pulse switches only those pixels preconditioned by application of the first ac bias so that a required pattern of pixels is displayed.

3. The display of claim 2 wherein the means for generating the ac bias are strobe waveforms applied to the m set of electrodes and data waveforms applied to the n set of electrodes.

Fig.1.

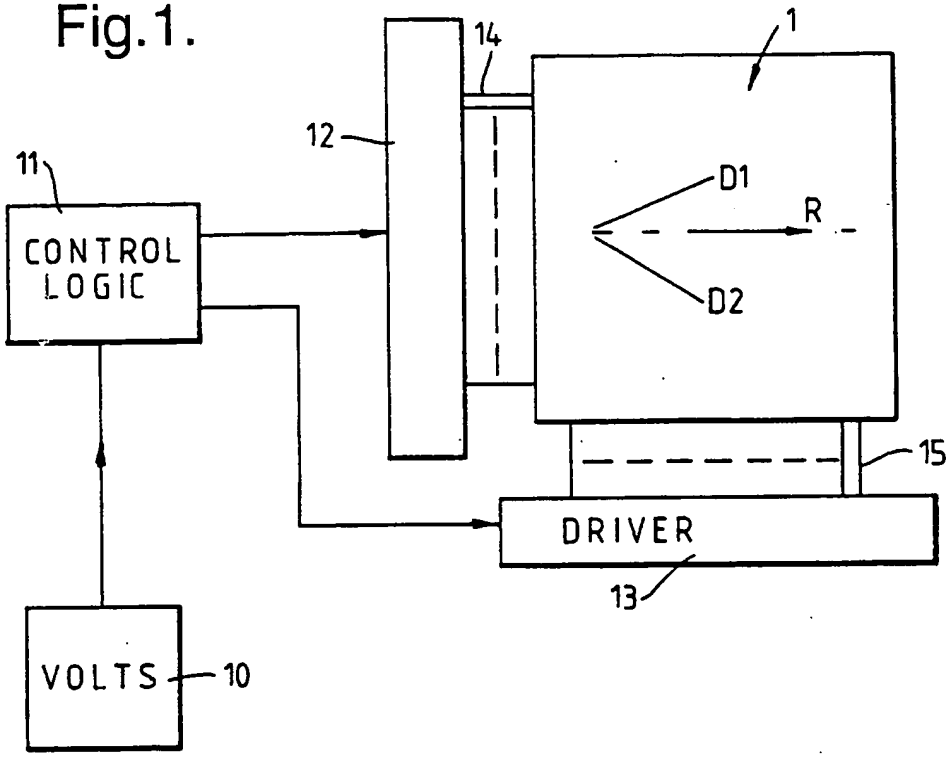

14
1
12
11
D1
R
CONTROL LOGIC
D2
15
DRIVER
13
VOLTS
10

Fig.2.

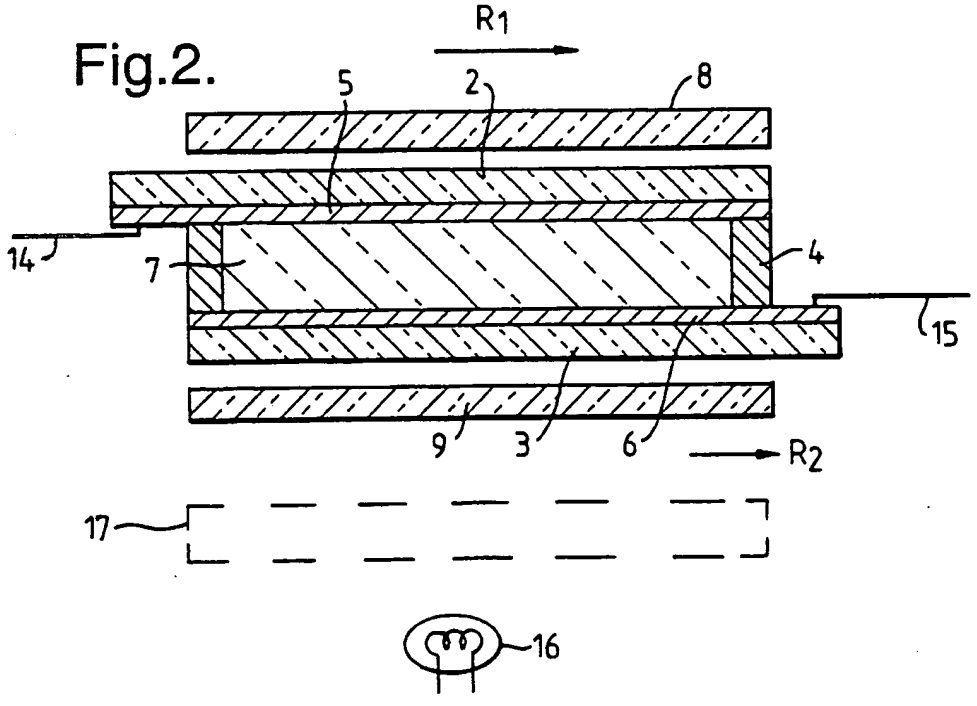
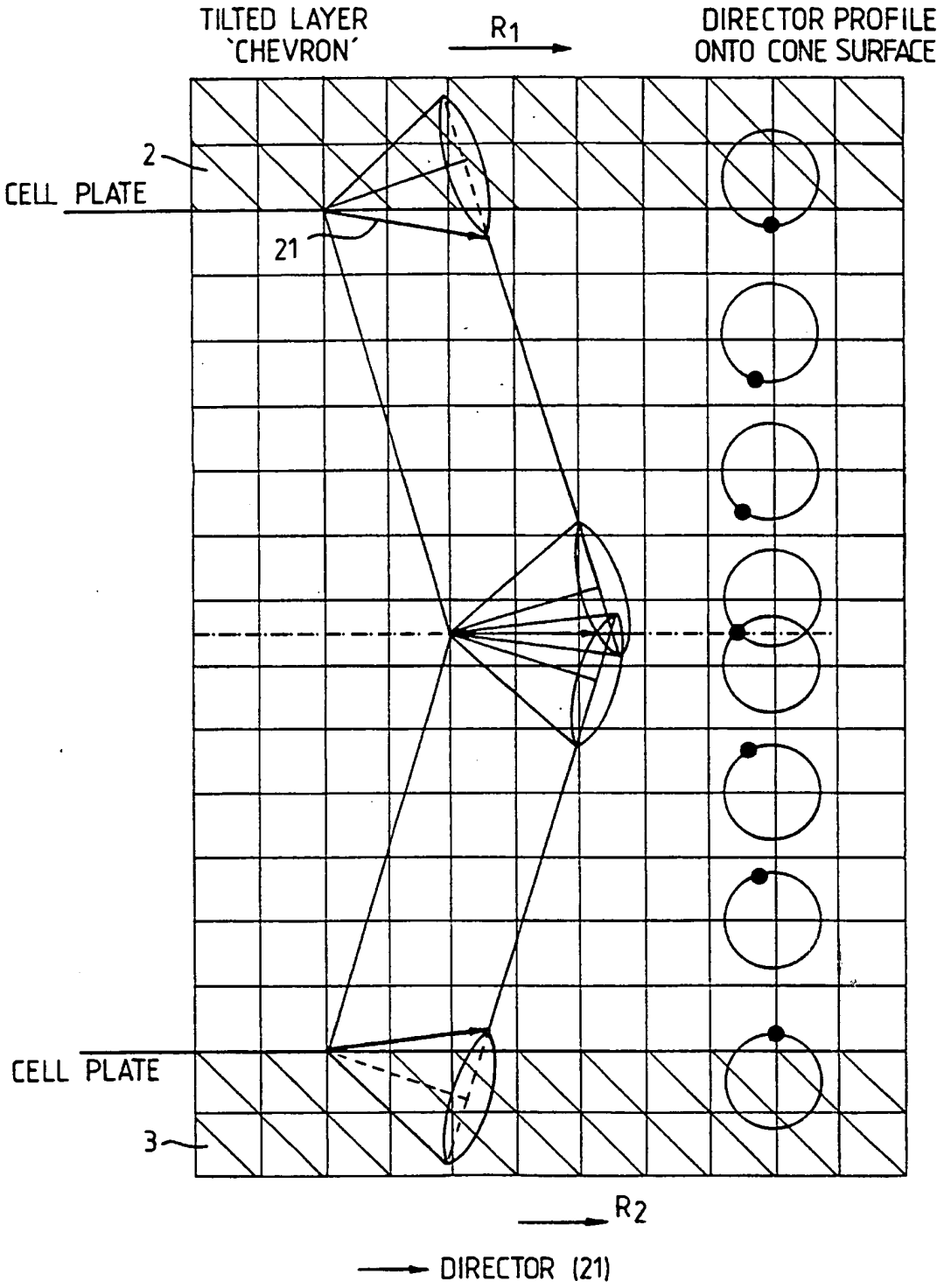

R1
5
2
8
14
7
4
15
9
3
6
R2
17
16

Fig.3.


TILTED LAYER
'CHEVRON'
R1
DIRECTOR PROFILE
ONTO CONE SURFACE
2
CELL PLATE
21
CELL PLATE
3
R2
DIRECTOR (21)

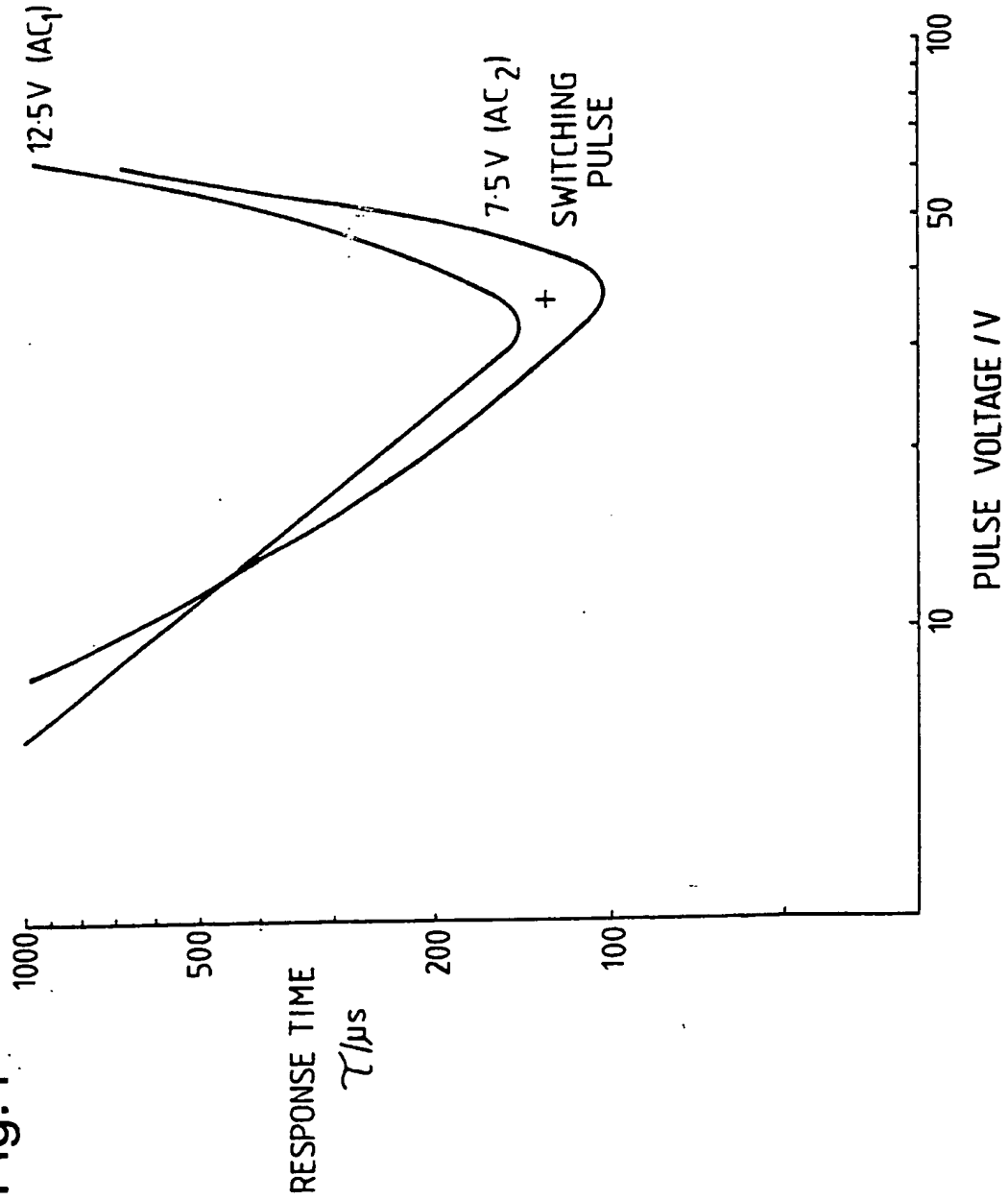
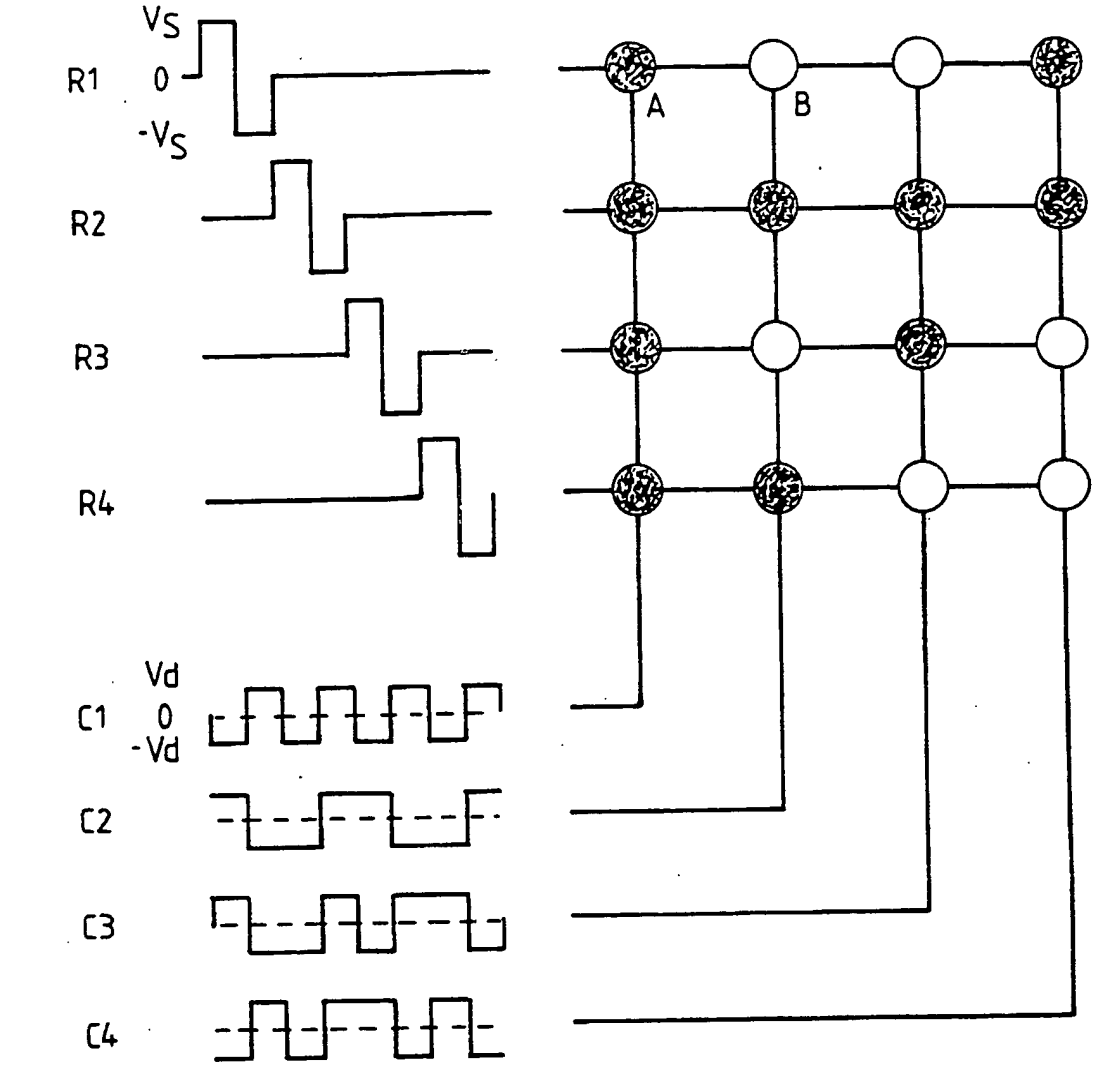
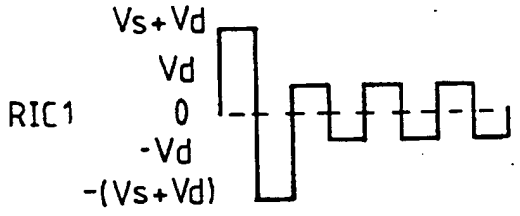

12·5 V (AC1)
7·5 V (AC2)
SWITCHING PULSE
+
1000
500
200
100
RESPONSE TIME
τ/μs
10
50
100
PULSE VOLTAGE / V

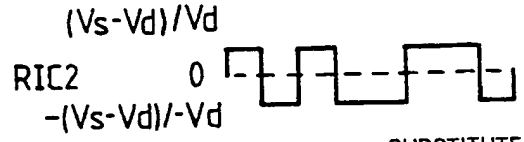
Fig.4

Fig.5.



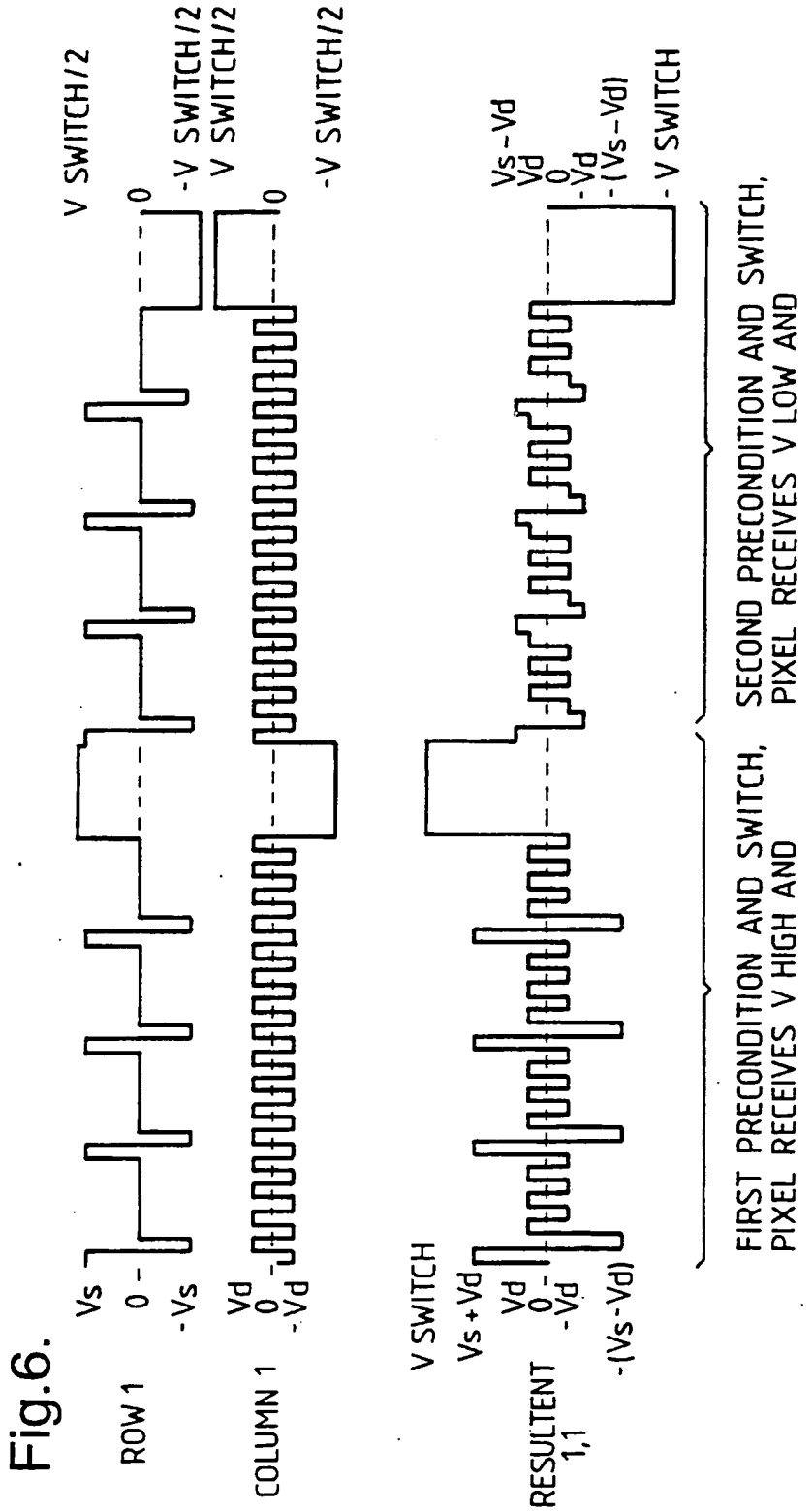


RESULTANT AT A (RIC1)



RESULTANT AT B [Vs-Vd]=[Vd] (RIC2)

Fig.6.


ROW 1
Vs
0
-Vs
COLUMN 1
Vd
0
-Vd
V SWITCH/2
0
-V SWITCH/2
V SWITCH/2
0
-V SWITCH/2
RESULTENT 1,1
V SWITCH
Vs+Vd
Vd
0
-Vd
-(Vs-Vd)
Vs-Vd
Vd
0
-Vd
-(Vs-Vd)
-V SWITCH
FIRST PRECONDITION AND SWITCH, PIXEL RECEIVES V HIGH AND IS NOT SWITCHED
SECOND PRECONDITION AND SWITCH, PIXEL RECEIVES V LOW AND IS SWITCHED

INTERNATIONAL SEARCH REPORT

Inter nal Application No
PCT/GB 94/00749

A. CLASSIFICATION OF SUBJECT MATTER
IPC 5 G09G3/36

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 5 G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP,A,0 337 780 (THRON EMI PLC) 18 October 1989 see Abstract see column 2, line 6 - column 3, line 9; figures 4,18,19 see column 9, line 28 - line 44 ---	1-3
A	EP,A,0 370 649 (STC PLC) 30 May 1990 see Abstract see column 6, line 27 - column 7, line 51; figures 3,4,6-8 see column 9, line 37 - column 12, line 2 --- -/--	1-3

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

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Date of the actual completion of the international search	Date of mailing of the international search report
13 July 1994	- 3. 08. 94

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+ 31-70) 340-2040, Tx. 31 651 epo nl, Fax (+ 31-70) 340-3016	Corsi, F

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INTERNATIONAL SEARCH REPORT

Inter mal Application No
PCT/GB 94/00749

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO,A,92 02925 (THE SECRETARY OF STATE FOR DEFENCE OF THE UK) 20 February 1992 cited in the application see Abstract see page 14, line 1 - page 16, line 21; figures 3-7	1-3
A	EP,A,0 306 203 (STC PLC) 8 March 1989 see Abstract see page 7, line 15 - line 53; figures 7,8 see page 9, line 28 - line 50; figures 11,12	1-3

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INTERNATIONAL SEARCH REPORT

Information on patent family members

Inter. nal Application No
PCT/GB 94/00749

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
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		ES-T-	2048836	01-04-94
		JP-A-	2204722	14-08-90
		US-A-	5128663	07-07-92
EP-A-0370649	30-05-90	GB-A-	2225473	30-05-90
		JP-A-	2187722	23-07-90
		US-A-	5018834	28-05-91
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		CN-A-	1058850	19-02-92
		EP-A-	0542804	26-05-93
		GB-A,B	2262831	30-06-93
		JP-T-	5509419	22-12-93
EP-A-0306203	08-03-89	DE-D-	3889606	23-06-94
		JP-A-	3020715	29-01-91
		NO-C-	173302	24-11-93
		US-A-	5047757	10-09-91